AN SOI PROCESS FOR FABRICATION OF SOLAR CELLS, TRANSISTORS AND ELECTROSTATIC ACTUATORS

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ABSTRACT

We have developed a new process for fabricating integrated, solar-powered microelectromechanical systems (MEMS) on a silicon-on-insulator (SOI) wafer. The intended applications for this process are autonomous microsystems, such as microrobots and distributed sensor networks. Two versions of the process have been created. The first combines solar cells and MEMS devices with NMOS transistors utilizing metal gates. This version has yielded solar cell efficiencies greater that 11%, a 200 cell array with an output of 88.5 V and transistor breakdown voltages above 25 V. Using this process, a fully integrated device has been demonstrated consisting of an electrostatic, gap-closing actuator being powered by an on-board solar cell array with the power being switched by an on-board buffer consisting of an NMOS inverter. The only external connections were ground and a 5 V control signal. A second version has also been developed which provides better solar cell performance and CMOS circuits utilizing polysilicon gates. This version has yielded solar cell efficiencies greater than 14%, a 90 cell array with an output over 50 V, and NMOS and PMOS devices with breakdown voltages greater than 50 V.

INTRODUCTION

The goal of this research project was to create an integrated process which would aid in the creation of autonomous microsystems. Two specific target applications are distributed sensor networks [1] and microrobots [2]. Devices like these are comprised of three types of components. These are power sources, circuits and MEMS devices. By using an integrated process, all of these components can be fabricated together on a single, monolithic chip, simplifying assembly and reducing the overall size of the device.

In order to meet the power needs of an autonomous microsystem, we chose solar cells because light is commonly available and solar cell technology is compatible with existing microfabrication. Possible technologies for creating photogenerators include single crystal silicon, amorphous silicon and gallium arsenide. These options lead to a number of viable integration schemes. The one chosen for this research combines single crystal silicon solar cells and high aspect ratio MEMS devices on an SOI wafer. Typically, single crystal silicon would be at a disadvantage to amorphous silicon and gallium arsenide because it requires a thicker cell to extract the majority of available power [3], but by integrating with the MEMS devices, the benefits of having high aspect ratio MEMS offsets the thickness penalty. Including back-filled isolation trenches in the SOI device layer, like those used by Brosnihan [4] allow a large number of solar cells to be wired in series to generate high voltages. These are especially well suited to driving electrostatic MEMS devices.

The final component of the microsystem which must be considered is the circuitry. Although the fabrication steps necessary to create the solar cells can be used to make basic circuit elements, it would not be practical to fabricate complex circuits in this process. A better scheme is to fabricate the control circuits in a standard CMOS process and use the circuit elements on the solar cell and MEMS chip as a buffer between the two. These buffers allow the low voltage control signals from the CMOS to direct the high voltage power from the solar cell arrays to the MEMS devices.

Until recently, literature on micro solar cell arrays has not been widely published. Research on gallium arsenide solar cell arrays has achieved an output of 100 V from a 120 cell array [5]. Using a single wavelength light source, an efficiency of 7% has been demonstrated. Another example used a 100 cell array of hydrogenated, amorphous silicon solar cells to power an off-chip electrostatic micromirror [6]. Based on the published results, the estimated efficiency achieved was 0.16%.

PROCESS DESCRIPTION

The fabrication of the integrated SOI process has four major stages. They are the SOI substrate fabrication, formation and back-filling of the isolation trenches, solar cell and circuit fabrication and the etching and release of the MEMS structures. Two versions of the process have been created. The first version, which will be described in detail in this section, uses the minimum processing steps necessary for solar cell fabrication to create the circuit elements. This allows the creation of NMOS transistors with metal gates. The second version adds more processing steps so that the circuit fabrication is similar to a standard CMOS process. The differences are explained after the NMOS process description.

SOI Substrate Fabrication. The SOI wafers used for this process were custom fabricated. The device wafers, which were boron doped with a bulk resistivity of 0.1 - 0.5 Ω-cm, were first implanted to create a highly doped region of boron at the bonding surface. A micron of oxide was then grown on both the device and handle wafers. They were fusion bonded and annealed at 1100°C in a steam environment. The device layer was then ground and polished to final thickness of 50 μm.

Formation and Back-Filling of the Isolation Trenches. A wet oxidation of the wafers created a

protective oxide layer over the silicon. The pattern for the 2 µm wide isolation trenches was then applied. After etching through the oxide, the trenches were etched through the device layer using a Surface Technology Systems (STS) deep reactive ion etcher (DRIE), as shown in Fig. 1a. A 0.5 µm thick layer of low pressure, chemical vapor deposited (LPCVD) low stress nitride (LSN) was then deposited onto the wafer, creating a lining on the trench walls. The remainder of the trenches were then filled with undoped LPCVD polysilicon (Fig. 1b). A blanket dry etch of the polysilicon and LSN removed the back-fill materials from the surface and a hydrofluoric acid (HF) strip removed the protective oxide (Fig. 1c).

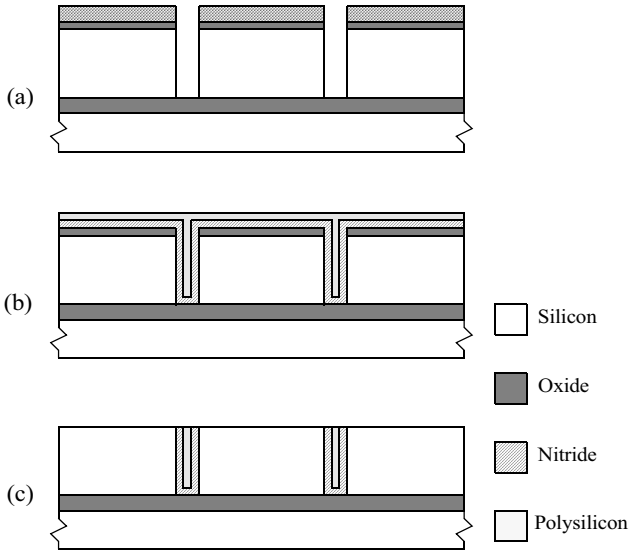

Figure 1. Process steps for the creation of back-filled isolation trenches. In (a), trenches are etched through protective oxide and device layer. They are filled with LSN and undoped polysilicon (b). Films are then removed from wafer surface in (c).

Solar Cell and Circuit Fabrication. The NMOS process required three implantations, an n- implant to create the pn junction for the solar cells, a p+ implantation for ohmic contact to the p type substrate, and an n+ implant for contact to the n- regions (n+ implant shown in Fig. 2a). Photoresist was used as a mask for these implantations. The target sheet resistances for the n- region was 300 Ω/square. The target parameter for the p+ and n+ regions was simply that the dopant concentration at the surface was greater than 10^{19} atoms/cm^3 so that a good ohmic contact was made with the aluminum.

The dopants were all driven-in during a single, three hour dry oxidation step performed at 1050°C (Fig. 2b). The resulting oxide layer was approximately 1000 Å thick. Contacts holes were etched and aluminum with 2% silicon was sputtered, patterned, plasma etched and sintered at 400°C (Fig. 2c). A 1 µm thick intermetal dielectric layer of LPCVD low temperature oxide (LTO) was deposited and a second layer of metal was applied which was used as a light blocking layer over the circuits. This layer consisted of 3000 Å of titanium and 500 Å of titanium nitride.

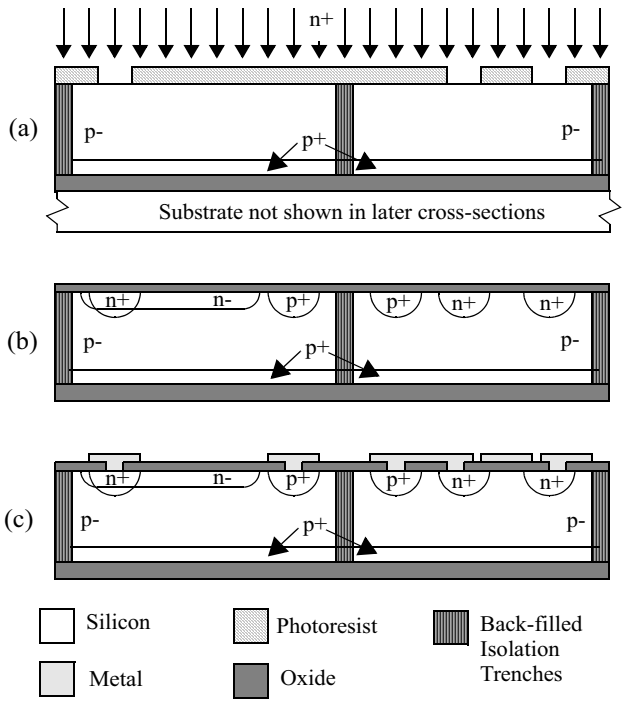

Figure 2. Process steps for creation of solar cells and circuits. Solar cell is shown on the left and an NMOS transistor is on the right. Three ion implantations create n-, n+ and p+ regions (a). In (b), a single oxidation step drives in the dopants . Contacts are etched and metal is sputtered and etched (c).

Etching and Release of MEMS structures. The final and most difficult stage was the etching and release of the MEMS structures. The etching was fairly straightforward, using DRIE, but sufficiently protecting the solar cells and circuits proved to be a much greater challenge. A blanket layer of boron doped, LPCVD silicon germanium provided the needed protection. The processing steps are shown in Fig. 3. First, the oxide was removed from above the structures areas. A 5000 Å layer of boron doped silicon germanium was deposited over the wafer (Fig. 3a). The pattern for the structure etch was then applied and etched using DRIE through both the germanium and the device layer (Fig. 3b). The photoresist was removed but the germanium layer was left in place during the concentrated HF release of the structures. The devices were rinsed to water and then put directly into 30% hydrogen peroxide at 90°C to dissolve the germanium. The samples were rinsed to methanol and dried using CO_2 critical point drying.

Many characteristics of silicon germanium make it especially well suited to this application. First, the low deposition temperature causes no negative effects on the performance of the solar cells and circuits. This also makes it safe to deposit even after low temperature metals, like aluminum, have been used on the wafer. Additionally, it provides an effective barrier to concentrated HF and is compatible with the SF_6 etch chemistry used to etch the MEMS structures. This allows it to be placed directly over the MEMS areas and etched along with them, eliminating

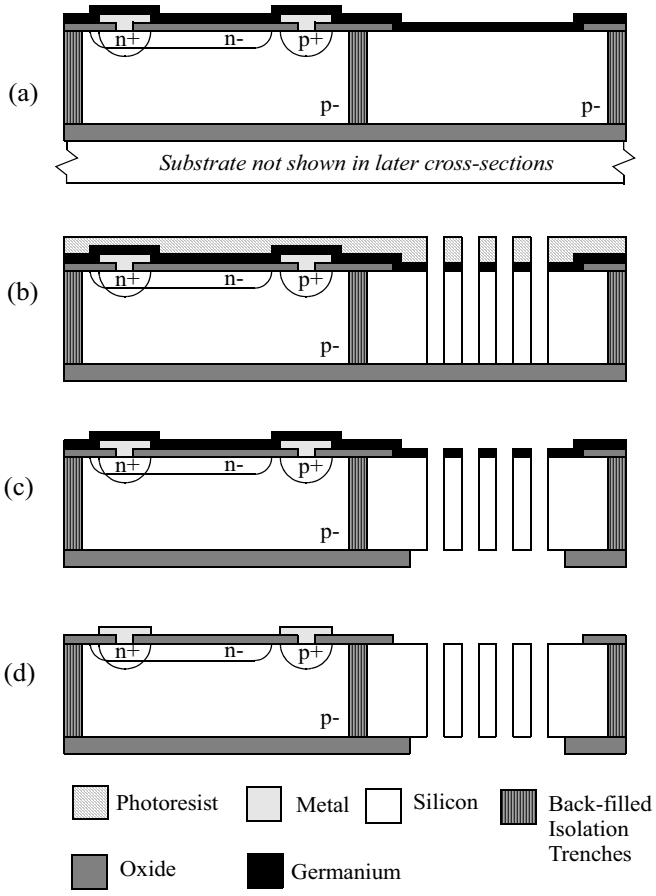

Figure 3. Processing steps for the etching and release of the MEMS structures. In (a), a blanket layer of boron doped germanium is deposited on the wafer. The structures are etched (b) and released (c) and the germanium is then removed (d).

the need for an extra mask step. Lastly, the easy removal in hydrogen peroxide simplifies its integration.

Using germanium as a protection layer did require one modification to the original process. It was found that if there were any areas of exposed aluminum when the germanium was deposited, the germanium would diffuse into the aluminum, leaving holes that led directly to the aluminum. The HF would quickly attack the aluminum through these holes and the solar cells and circuits would be ruined. Tests showed that this diffusion did not occur with either titanium or titanium nitride, so the aluminum top metal layer was replaced with a titanium/titanium nitride stack.

CMOS Process Differences. In order to improve the performance of the circuit elements, the CMOS version of the process was developed. Whereas the parameters for the NMOS process had been chosen with only the solar cells in mind, the CMOS process was developed to balance the needs of both solar cells and circuits. Therefore, the solar cell and circuit stage of the process more closely resembles a standard CMOS process, including the use of self-aligned polysilicon gates. The doping levels were also modified to provide higher breakdown voltages and better control over the threshold voltages Another difference was that the isolation trench stage of the process was done after the solar cells and circuits but before the metal layers were applied.

DESIGN

Solar Cell Design. The initial design for the solar cells was based on previous work on SOI solar cells [7]. In that research, single crystal silicon solar cells were fabricated on a 50 μm thick SOI wafer. The design did not include any means of isolating solar cells, so high voltage outputs could not be obtained. The solar cell design for the research presented here includes isolation from the surrounding silicon through the use of back-filled isolation trenches, a highly doped back surface field (BSF), and an antireflective oxide layer. A fabricated solar cell from the NMOS process can be seen in Fig. 4.

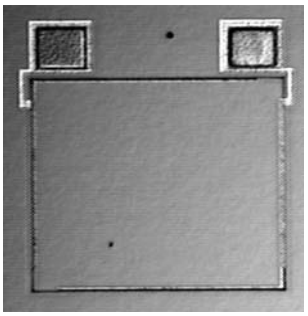

Figure 4. Single test solar cell measuring 400 μm x 400 μm from the NMOS version of the process.

The BSF is a highly doped region at the bottom of the device layer, just above the interface between the device layer and the bonding oxide layer. It can be seen in Fig. 2. The dopant for this regions is the same as the bulk of the device layer. Its presence improves the efficiency by reducing the amount of recombination that occurs at that interface.

By controlling the thickness of the passivating oxide layer which is grown on top of the solar cells, an antireflective effect can be achieved. By selecting the thickness, d, according to $d = \frac{\lambda}{4n}$ where λ is the dominant wavelength and n is the refractive index of the oxide, destructive interference can be created. The thickness of the passivating oxide layer was chosen to be ~1000 Å to minimize reflection of the peak wavelength of sunlight, ~575 nm.

To generate high voltage outputs, a number of cells were simply wired in series. The main test array for the NMOS process, shown in Fig. 5, consisted of 200 cells, each one measuring 400 μm x 400 μm. The cells were separated into groups of 20 with wire bond pads situated so that they could be easily wired to provide different outputs.

Circuit Design. As previously mentioned, two separate versions of the process have been demonstrated which differ in the circuit capabilities. Designing within the capabilities of the NMOS process, two buffer designs were fabricated. The first was simply an NMOS inverter with a pull-up

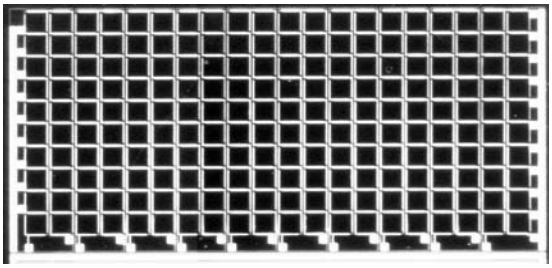

Figure 5. Variable output solar cell array with 200 cells, fabricated in the NMOS version of the process. Each cell measures 400 µm x 400 µm.

resistor. The second buffer design has two stages with the output being connected to both the ground and the supply line through two separate NMOS transistors. An NMOS inverter with pull-up resistor is then used to create the complement to the input signal so that the two transistors are fed opposite signals, as shown in Fig. 6. An isolation trench is placed around the supply line transistor.

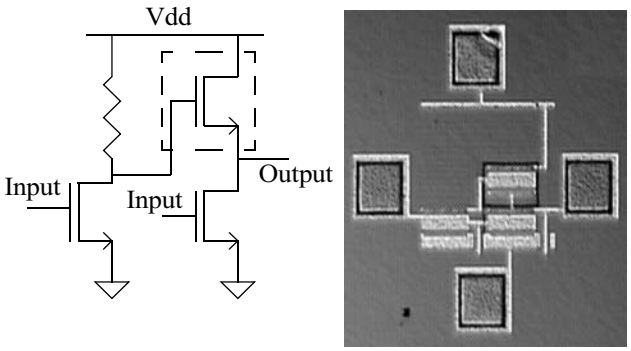

Figure 6. Two-stage buffer design from the NMOS process. The dotted line in the schematic indicates the location of an isolation trench, which can be seen in the picture to the right. For reference, the bond pads are 125 µm square.

The improved capabilities of the CMOS version of the process allow a much more sophisticated buffer to be achieved. The resulting voltage translator circuit is shown in Fig. 7. The compliment to the input signal is created and both are fed into a variant of a cross coupled inverter. A significant benefit to this design is that zero static current is required to operate it.

Electrostatic Actuator Design. The electrostatic actuators that were used for demonstration of the fully integrated process were based on a previously demonstrated inchworm motor [8]. Test actuators were made which represented both the clutch and drive stages of the inchworm motor. The actuators use gap closing actuators with an initial gap of 2 µm. They can be seen in Fig. 8.

RESULTS

The solar cells were tested under both microscope and solar illumination. The microscope provided a consistent light source for comparing cells but because the intensity and spectrum were unknown, efficiency estimates could not be made. For solar illumination, the cells were packaged and wire bonded so that they could be easily tested outside. By

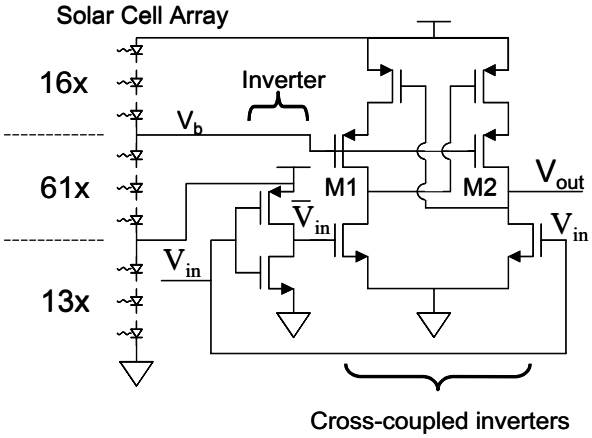

Figure 7. Voltage translator design fabricated using the CMOS version of the process.

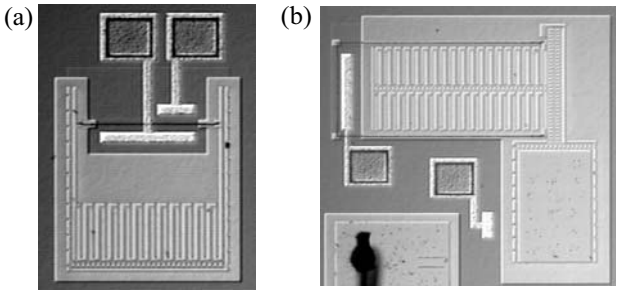

Figure 8. Electrostatic actuators used to demonstrate the integrated process. Inchworm clutch stage is shown in (a) and drive stage is shown in (b).

estimating the input power from the sun, the efficiencies for the cells could be calculated.

The data in Table 1 summarizes the performance for all of the cells in a 200 cell array, as shown in Fig. 5. This array was fabricated using the NMOS version of the process. The first ten rows contain the data for each of the 10 individual arrays, containing 20 cells each. These arrays were then wired in series to provide the data in the final row. This data was taken under solar illumination with an estimated Air Mass (AM) of 1.71. From this value, the incident power was estimated to be 758 $\mu W/mm^2$.

The solar cells fabricated in the CMOS version of the process had even better performance. An array with 90 cells wired in series, each measuring 150 µm square, produced an open circuit voltage over 50 V. An individual cell of the same size had an estimated efficiency of 14.3% under AM2.0 illumination.

The NMOS process was used to make transistors with lengths of 20 and 30 µm. The average threshold voltage for 20 µm devices was 2.39 V and for 30 µm devices, it was 2.25 V. The average breakdown voltages were 27.2 V and 28.0 V, respectively. The breakdowns never caused permanent damage to the transistors, indicating that the breakdown had not occurred across the gate oxide.

The performance of the two buffer designs from the NMOS process are shown in Fig. 9. The two stage buffer is

Table 1: Solar cell data for 200 cell array

Number of cells in series	Open Circuit Voltage (V)	Max. Power (W)	Efficiency (%)
20	8.4	181	7.5
20	8.6	190	7.8
20	11.1	275	11.3
20	11.3	283	11.7
20	11.2	274	11.3
20	11.2	281	11.6
20	10.7	271	11.2
20	9.1	199	8.2
20	10.1	255	10.5
20	11.3	282	11.6
200	88.5	2010	8.3

the one shown in Fig. 6. The supply voltage for both sets of data was 25 V. When the output was high, both buffers exhibited a difference between the supply voltage and the output voltage of 3.3 V. The simple buffer turned off more abruptly than the two stage buffer, but both switched at a higher point than is desirable for easy integration with a standard CMOS control chip.

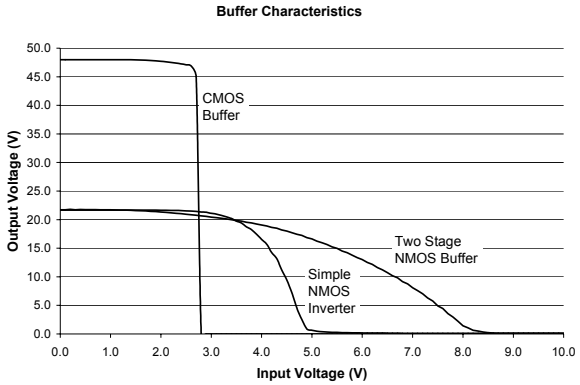

Figure 9. Buffer characteristics. The supply voltages were 25 V for the NMOS buffers and 48 V for the CMOS buffer.

With the improvements made in the CMOS process, the transistors and buffers performed significantly better. The breakdown voltages of the NMOS transistors were increased to more than 50 V. The PMOS transistors had even higher breakdown voltages, ranging between 65 and 100 V, depending on the design. The performance of the voltage translator (Fig. 7) is shown in Fig. 9. The curve shows that when the input voltage was zero, there was no difference between the supply and output voltages. Additionally, the switch occurred abruptly and at a low enough voltage for a standard CMOS chip.

The complete integration of an electrostatic actuator being powered by an on-chip solar cell array and controlled by an on-chip buffer was demonstrated using the NMOS version of the process. The successful combination consisted of a 30 cell array, the two-stage buffer (Fig. 6) and the drive test actuator (Fig. 8b). The voltage needed for actuation was approximately 15 V. The solar cell array was illuminated by a halogen lamp and produced slightly more than 15 V. When the input voltage of the buffer was zero, the actuator would pull in to the stops. At an input voltage of 4.5 V, the actuator was completely released.

CONCLUSIONS

We have developed and demonstrated an integrated process which provides for the fabrication of high voltage solar cell arrays, high aspect ratio electrostatic actuators and high voltage buffers on an SOI wafer. The process is intended for the creation of autonomous microsystems which would benefit from the power generation of the solar cell arrays. The process has been used to fabricate solar cells with efficiencies greater than 14% and solar cell arrays with output voltages above 88 V. Circuits have been demonstrated which can act as an effective buffer between a low voltage CMOS chip and the high voltage solar cells and actuators. The complete integration of an electrostatic actuator being powered by an on-chip solar cell array and switched by an on-chip buffer has been shown.

Acknowledgements

We would like to thank the staff of the UC Berkeley Microfabrication Laboratory for all of their help during the completion of this research.

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